BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features and other aspects of the invention are explained in the following description taken in connection with the accompanying drawings, wherein:

FIG. 1 is a simplified cross-sectional view of an integrated circuit package according to one embodiment of the present invention;

FIG. 2 is a simplified cross-sectional view of an integrated circuit package according to a second embodiment of the present invention;

FIG. 3 is a simplified bottom view of an integrated circuit package according to embodiments of the present invention;

FIGS. 4A - 4H show one example of steps performed in assembly of embodiments of an integrated circuit package of the present invention.

FIGS. 5A - 5I show another example of steps performed in assembly of embodiments of an integrated circuit package of the present invention.

FIG. 6 is a simplified cross-sectional view of an integrated circuit package assembly including an integrated circuit package as shown in FIG. 2 and another integrated circuit package.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Various embodiments of the integrated circuit package and various examples of methods for manufacturing integrated circuit packages according to the present invention will now be described with reference to the drawings.

FIGS. 1 and 2 show certain components of integrated circuit packages according to embodiments of the present invention. The integrated circuit packages depicted in FIGS. 1 and 2 each generally include a substrate 101, a semiconductor die

103 and an encapsulant 105. The substrate 101 may be made of either a rigid material (*e.g.*, BT, FR4, FR5 or ceramic) or a flexible material (*e.g.*, polyimide), and may have circuit traces 112 onto which a semiconductor die 103 may be interconnected using, for example, wire bonding techniques or tape automated bonding. In the embodiment shown in FIG. 1, the package measures about 1.0 mm thick (shown as dimension "a" in FIG. 1) and about 35 mm wide (shown as dimension "b" in FIG. 3). The width dimension of certain other embodiments may vary from 7 mm to 50 mm. However, such dimensions are provided only as non-limiting examples of certain embodiments of the present invention.

As shown in FIG. 2, external terminals of one embodiment of the present invention may include an array of solder balls 106. In such an embodiment, the solder balls 106 may function as leads capable of providing power, signal inputs and signal outputs to the semiconductor die 103. Such a configuration may be referred to as a type of ball grid array. Absent the solder balls 106, such a configuration may be referred to as a type of land grid array, as shown in FIG. 1.

In one embodiment, traces 112 may be embedded photolithographically into the substrate 101, and are electrically conductive to provide a circuit connection between the semiconductor die 103 and the substrate 101. Such traces 112 may also provide an interconnection between input and output terminals of the semiconductor die 103 and external terminals provided on the package. In particular, the substrate 101 of the embodiment shown in FIG. 1 may have a multi-layer circuit trace 112 made of copper. The substrate 101 shown in FIG. 1 has vias 110 which may be drilled into it to connect the top and bottom portions of each circuit trace 112. Such vias 110 may be

plated with copper to electrically connect the top and bottom portions of each trace 112. The substrate 101 shown in FIG. 1 may also have a solder mask on its surface. The solder mask of one embodiment electrically insulates the substrate and reduces wetting (*i.e.*, reduces unwanted flow of solder into the substrate 101).

As shown in FIGS. 1-3, the substrate 101 is designed with a cavity 120 made through the base material with sufficient clearance to accommodate the specific size of semiconductor die 103 used in the package.

One embodiment may include a conductive trace 112 in the form of a ring around the cavity 120 in the substrate 101. Such a ring-shaped conductive trace 112 may be connected to the top surface of the substrate 101 by means of electrically conductive vias 110. Such an arrangement may allow a heat slug 108 to be electrically connected to the semiconductor die 103 by the way of wire bonding 104, thereby resulting in a ground plane surface beneath the semiconductor die 103, which may enhance the electrical characteristics of the package.

In a preferred embodiment shown in FIG. 2, the encapsulant material 105 does not extend to the package edge. In such an embodiment, electrically conductive vias 110 connect traces 112 from the top surface of the package to corresponding pads 113 on the side of the package opposite to the solder ball attachment.

Example methods of manufacturing embodiments of the integrated circuit packages will now be described with reference to the drawings, in particular, FIGS. 4A-4H and FIGS. 5A-5I. FIG. 4A shows a step in the manufacture of one type of the integrated circuit package showing a substrate 101 with a cavity 120. The substrate 101 may be produced in a form to accommodate standard semiconductor manufacturing

equipment and process flows, and may also be configured in a matrix format to accommodate high-density package manufacturing. FIG. 5A depicts a step in another process for manufacturing integrated circuit packages, and shows a substrate 501 with a number of cavities 520-1, 520-2.

As shown in FIG. 4B, a tape 102 with adhesive material on at least one side is applied to the bottom side of the substrate 101, and may be applied in strip form to accommodate a number of substrates. The tape 102 may be, for example, a high temperature stable polyimide with an adhesive material on at least one surface. FIG. 5B depicts a tape 502 having its adhesive material on the surface which interfaces with the bottom of the substrate 501. In one embodiment, the adhesive material has a contact sticking characteristic such that a semiconductor die 103 placed into contact with the adhesive material will stick to the tape 502. In this embodiment, however, the adhesive material is such that no adhesive residue is left on the substrate 101 when the tape 502 is removed.

As shown in FIG. 4C, a semiconductor die 103 may then be mounted or otherwise attached to the tape 102 through the cavity 120 in the substrate 101. FIG. 5C depicts a number of semiconductor dies 503-1, 503-2 mounted or otherwise attached to the tape 502 through each of the cavities 520-1, 520-2 of the substrate 501.

As shown in FIG. 4D, the semiconductor die 103 may then be interconnected to routing traces 112 of the substrate 101 by a gold thermo-sonic wire bonding technique. In such an embodiment, gold wires 104 may interconnect the semiconductor die 103 to traces 112 of the substrate 101. FIG. 5D depicts the

semiconductor dies 503-1, 503-2 being interconnected to routing traces by, e.g., a gold thermo-sonic wire bonding technique.

As shown in FIGS. 4E and 5E, after wire bonding, the substrate 101, 501 may be encapsulated. The encapsulant material 105, 505 may be an epoxy based material applied by, for example, either a liquid molding encapsulation process or a transfer molding technique. To manufacture the embodiment of an integrated circuit package shown in FIG. 1, the substrate 101 is fully encapsulated on one side. To manufacture another embodiment of an integrated circuit package (shown in FIG. 2), the substrate 101 is encapsulated only in the semiconductor die 130 and wire bond area, leaving much of the surface of the substrate 101 opposite to the solder ball area free of encapsulant material 105. After an encapsulation process, the tape 102, 502 may then be removed from the package subassembly as shown in FIGS. 4F and 5F.

As shown in FIG. 4G, solder balls 106 may then be attached to traces 112 of the substrate 101 using, for example, a reflow soldering process. In another example method of manufacture, FIG. 5G depicts solder balls 506 being attached to traces 512 of the substrate 501. The solder balls 106, 506 may be made of a variety of materials including lead (Pb) free solder.

As shown in FIG. 4H, after solder ball attachment, a heat slug 108 may be attached to the exposed surface of the semiconductor die 103 and the area surrounding the cavity 120 in the substrate 101 using a thermally conductive adhesive material 107 such as epoxy. The adhesive material 107, may also be electrically conductive, such as silver-filled epoxy. FIG. 5H depicts attachment of a heat slug 508 to each semiconductor

die 503 only. However, an alternative heat slug, such as the one depicted in FIG. 4H, may also be attached to one or more semiconductor dies 503.

As shown in FIG. 5I, after such heat slug attachment, the integrated circuit packages may be singulated into individual units using, e.g., a saw singulation or punching technique.

FIG. 6 shows an integrated circuit package assembly according to an embodiment of the present invention. As depicted in FIG. 6, such an embodiment includes two integrated circuit packages stacked one on top of the other and attached to one another by solder balls 106. The integrated circuit package assembly shown in FIG. 6 includes two packages of the embodiment shown in FIG. 2 and a heat slug 108. Another embodiment of an integrated circuit package assembly according to the present invention may include two or more integrated circuit packages without a heat slug 108. Other embodiments of integrated circuit package assemblies according to the present invention may include integrated circuit packages other than the embodiments specifically shown in FIG. 6. As shown in FIGS. 1, 2, and 6, the substrate 101 of certain embodiments of integrated circuit packages and assemblies may contain electrically conductive traces 112 on an upper surface of the substrate 101 to facilitate electrical coupling with a second integrated circuit package.

The heat slug 108 shown in FIG. 6 may provide a thermal path between a semiconductor die 103 and the environment. In the embodiment shown in FIG. 6, the heat slug 108 may be aligned with and positioned below the bottom surface of the semiconductor die 103 such that the heat slug 108 may contact or thermally couple with an external device such as, e.g., a printed circuit board 200. The heat slug 108 is

preferably made of a thermally conductive material such as copper or copper alloy. The heat slug 108 may be sized and configured for use in a specific package arrangement such that, in certain embodiments, the heat slug 108 contacts another type of external device (e.g., an integrated circuit package) to which a package is attached. The heat slug 108 may be plated with solder or some other appropriate metal to enhance the reflow of solder to the surface of the heat slug 108. The opposite side of the heat slug 108 may also be oxide coated to enhance the adhesion to the encapsulant material 105.

Although specific embodiments of integrated circuit packages, integrated circuit package assemblies, and methods of manufacturing integrated circuit packages have been shown and described, it is to be understood that there are other embodiments which are equivalent to the described embodiments. Moreover, although a particular order of certain manufacturing steps has been discussed, it is to be understood that aspects of the invention are not limited to the particular order disclosed. The scope of the invention is not to be limited by the specific embodiments and examples depicted and described herein, but only by the claims.